FIG. 1

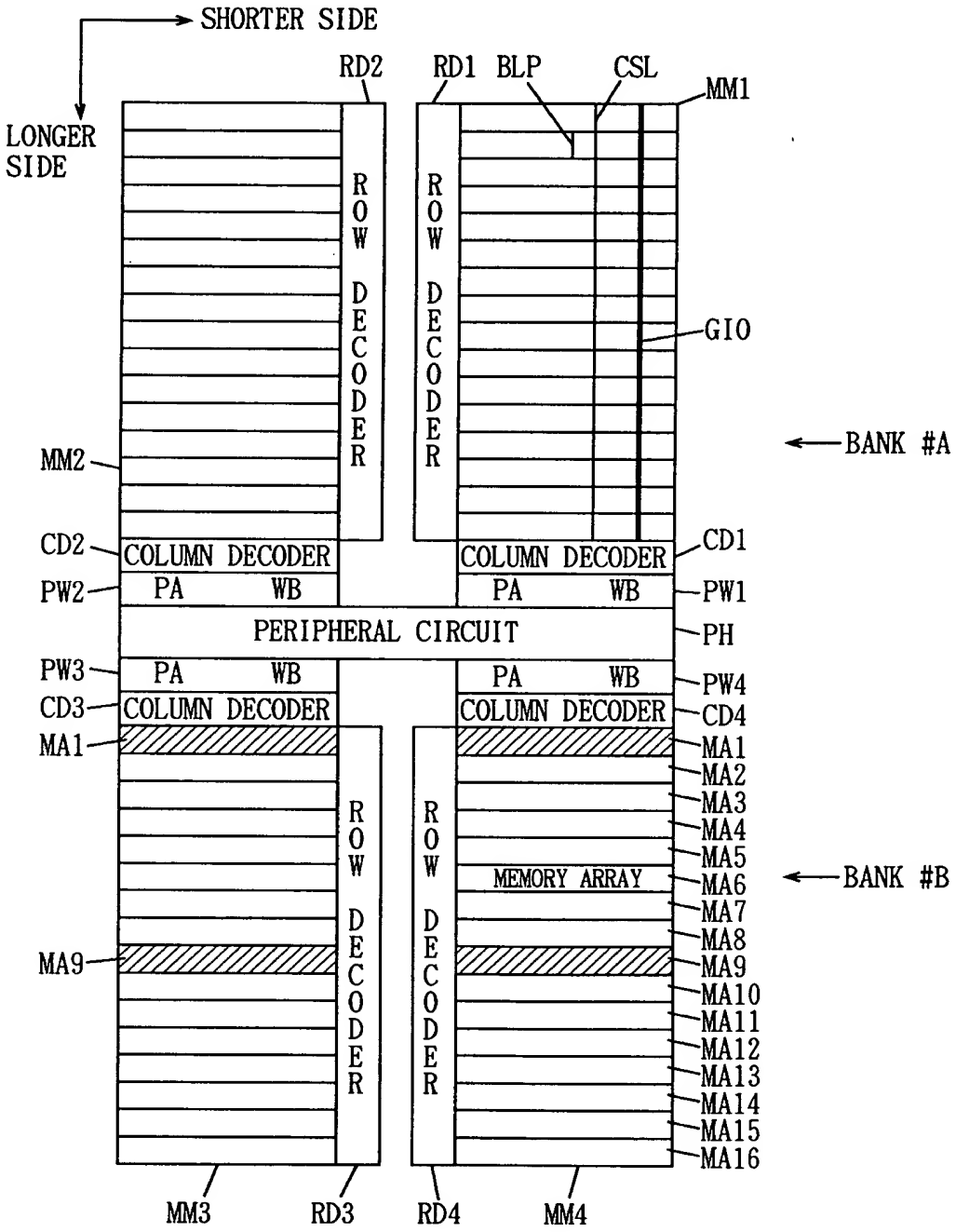

SHORTER SIDE
LONGER SIDE
RD2
RD1
BLP
CSL
MM1
GIO
MM2
BANK #A
CD2
CD1
COLUMN DECODER
COLUMN DECODER
PW2
PA
WB
PA
WB
PW1
PERIPHERAL CIRCUIT
PH
PW3
PA
WB
PA
WB
PW4
CD3
COLUMN DECODER
COLUMN DECODER
CD4
MA1
MA1
MA2
MA3
MA4
MA5
MEMORY ARRAY
MA6
BANK #B
MA7
MA8
MA9
MA9
MA10
MA11
MA12
MA13
MA14
MA15
MA16
ROW DECODER
ROW DECODER
ROW DECODER
ROW DECODER
MM3
RD3
RD4
MM4

FIG. 2

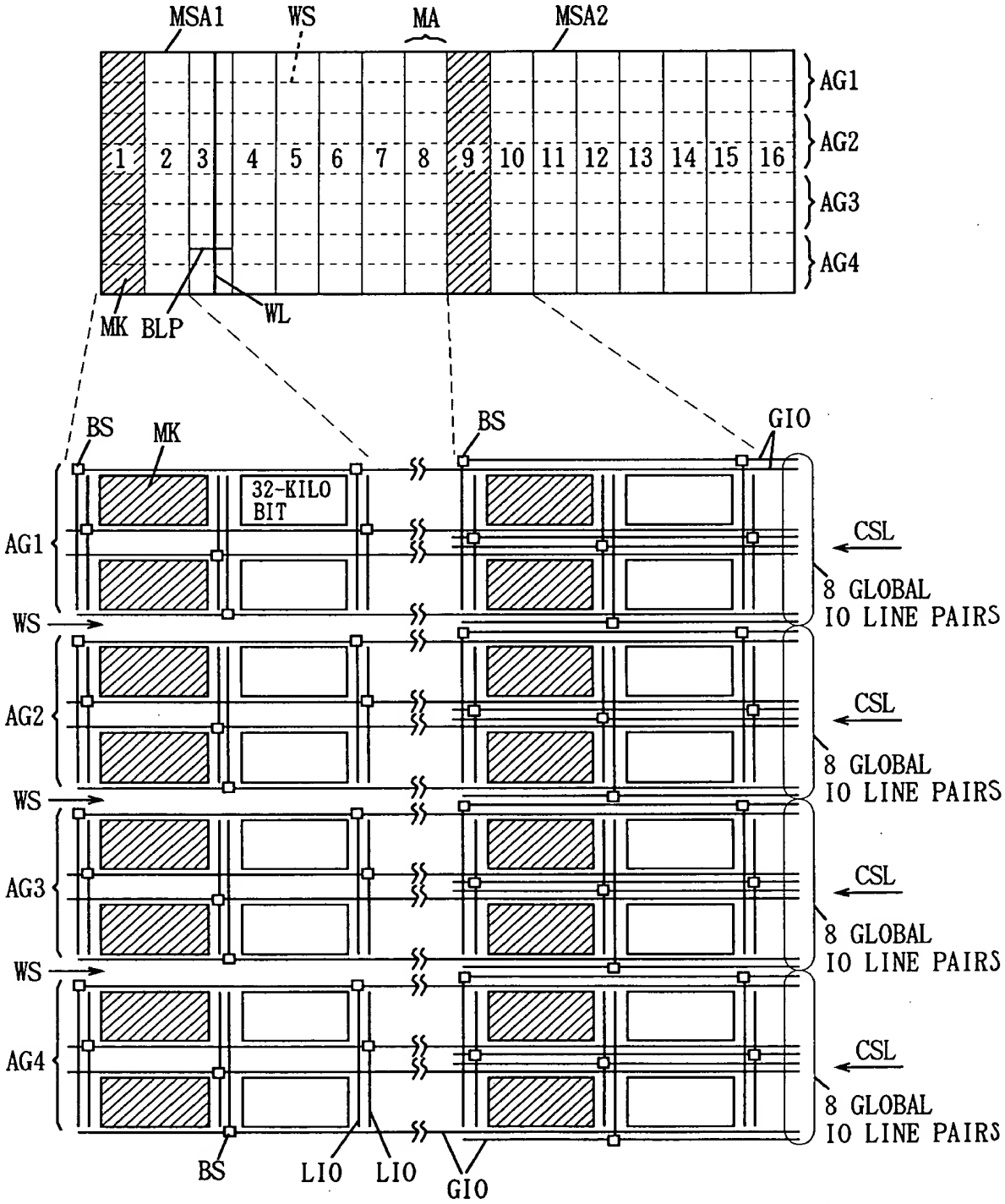

MSA1
WS
MA
MSA2
AG1
AG2
AG3
AG4
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
MK
BLP
WL
BS
MK
BS
GIO
32-KILO BIT
CSL
8 GLOBAL IO LINE PAIRS
WS
BS
LIO
LIO
GIO

FIG. 3

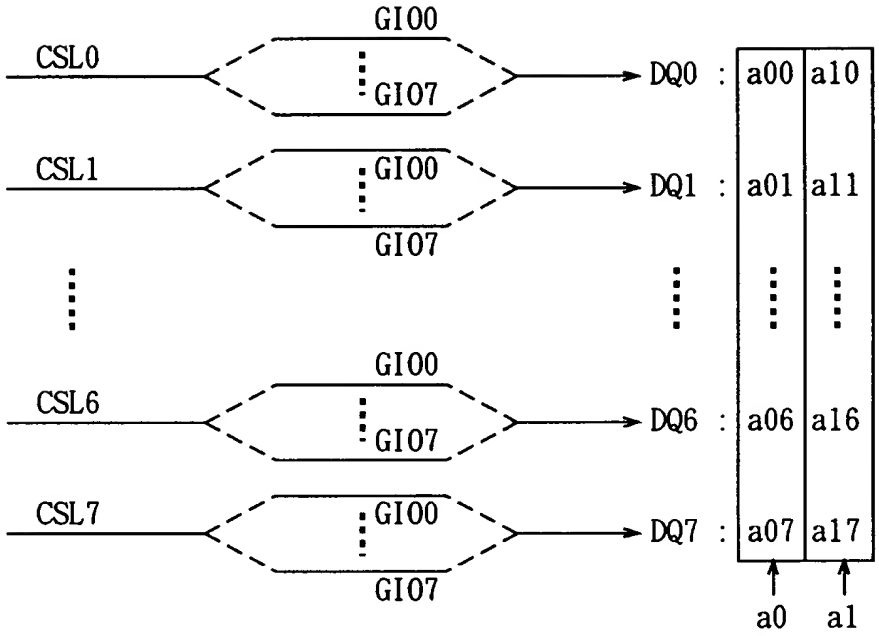

GI00
CSL0
GI07
DQ0 : a00 a10
GI00
CSL1
GI07
DQ1 : a01 a11
GI00
CSL6
GI07
DQ6 : a06 a16
GI00
CSL7
GI07
DQ7 : a07 a17
a0
a1

FIG. 4

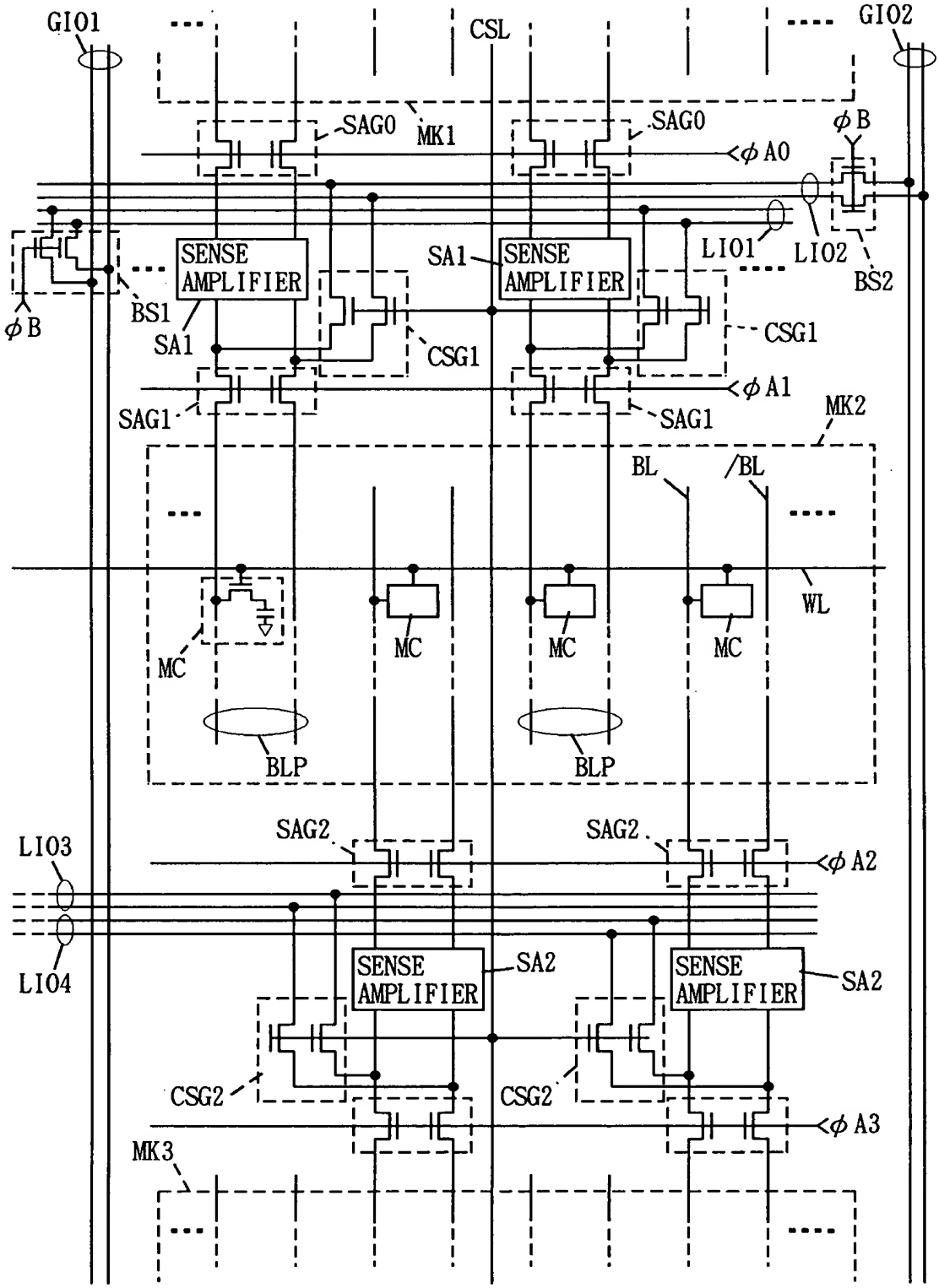
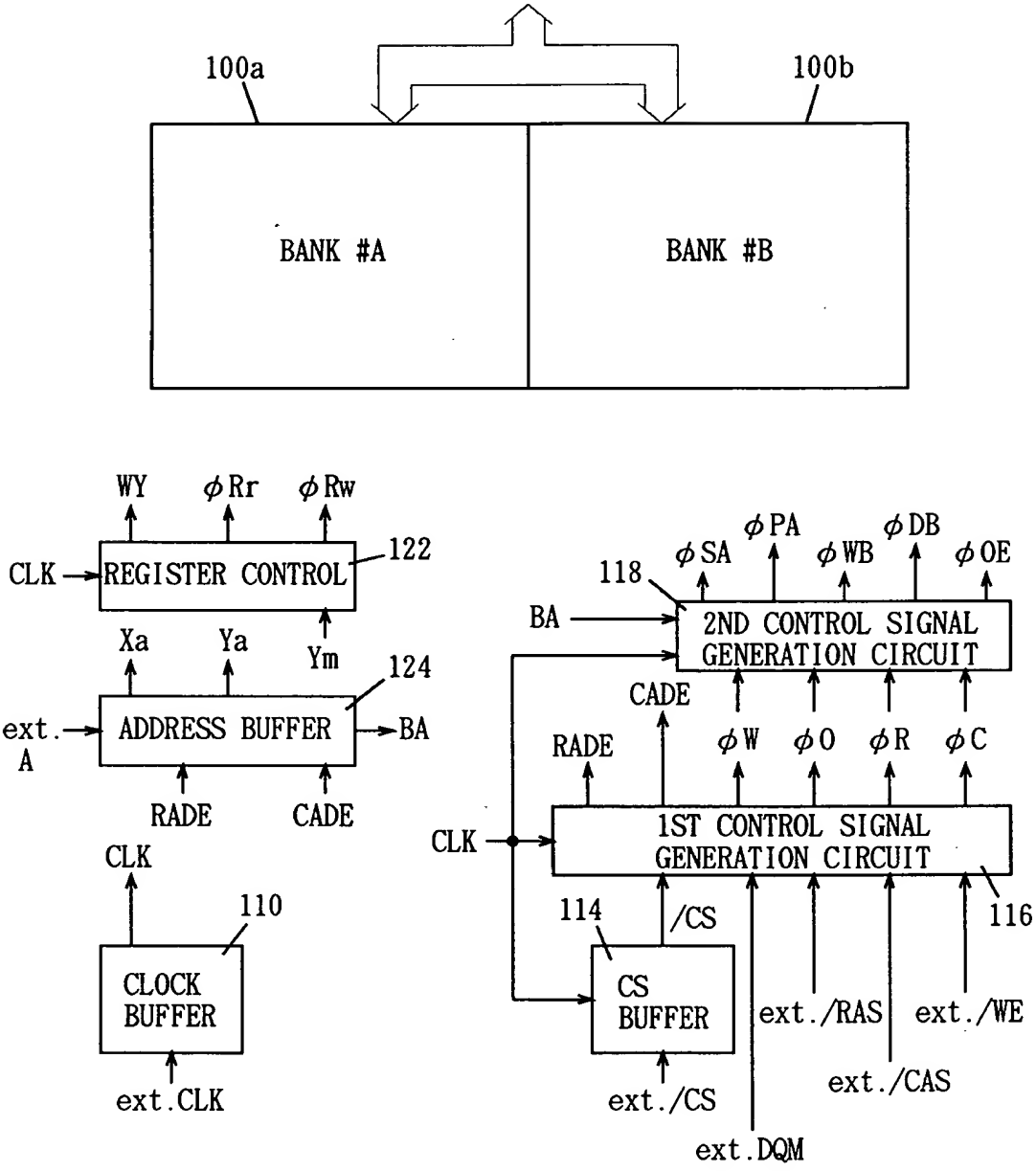

GIO1
CSL
GIO2
SAG0
MK1
SAG0
φB
φA0
SENSE AMPLIFIER
SA1
SENSE AMPLIFIER
LIO1
LIO2
BS2
φB
BS1
SA1
CSG1
CSG1
φA1
SAG1
SAG1
MK2
BL
/BL
WL
MC
MC
MC
MC
BLP
BLP
LIO3
SAG2
SAG2
φA2
LIO4
SENSE AMPLIFIER
SA2
SENSE AMPLIFIER
SA2
CSG2
CSG2
φA3
MK3

FIG. 5


100a
100b
BANK #A
BANK #B
WY
φRr
φRw
CLK
REGISTER CONTROL
122
Xa
Ya
Ym
124
ext.
A
ADDRESS BUFFER
BA
RADE
CADE
CLK
110
CLOCK
BUFFER
ext.CLK
φPA
φDB
φSA
φWB
φOE
118
BA
2ND CONTROL SIGNAL
GENERATION CIRCUIT
CADE
RADE
φW
φO
φR
φC
CLK
1ST CONTROL SIGNAL
GENERATION CIRCUIT
114
/CS
116
CS
BUFFER
ext./RAS
ext./WE
ext./CS
ext./CAS
ext.DQM

PH

FIG. 6

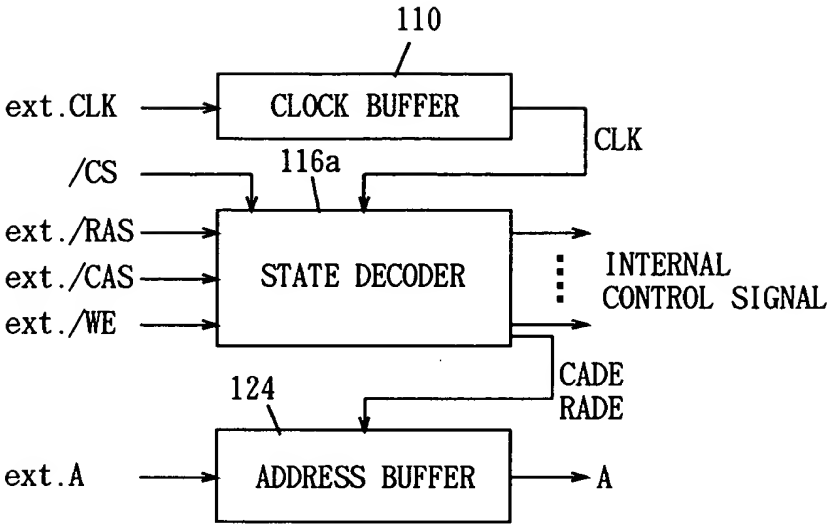

110
ext.CLK
CLOCK BUFFER
CLK
/CS
116a
ext./RAS
ext./CAS
ext./WE
STATE DECODER
INTERNAL
CONTROL SIGNAL
CADE
RADE
124
ext.A
ADDRESS BUFFER
A

FIG. 7

FUNCTION	/CS	/RAS	/CAS	/WE	DQM
ROW ADDRESS STROBE AND ARRAY ACTIVATION	L	L	H	H	—
COLUMN ADDRESS STROBE AND READ	L	H	L	H	—
COLUMN ADDRESS STROBE AND WRITE	L	H	L	L	—
PRECHARGE / SELF REFRESH END	L	L	H	L	—
REFRESH / SELF REFRESH START	L	L	L	H	—
SET MODE REGISTER	L	L	L	L	—
WRITE ENABLE / OUTPUT ENABLE	—	—	—	—	L
WRITE MASK / OUTPUT DISABLE	—	—	—	—	H
NO CHANGE	L	H	H	H	—
IGNORE /RAS, /CAS & /WE	H	×	×	×	—

FIG. 8

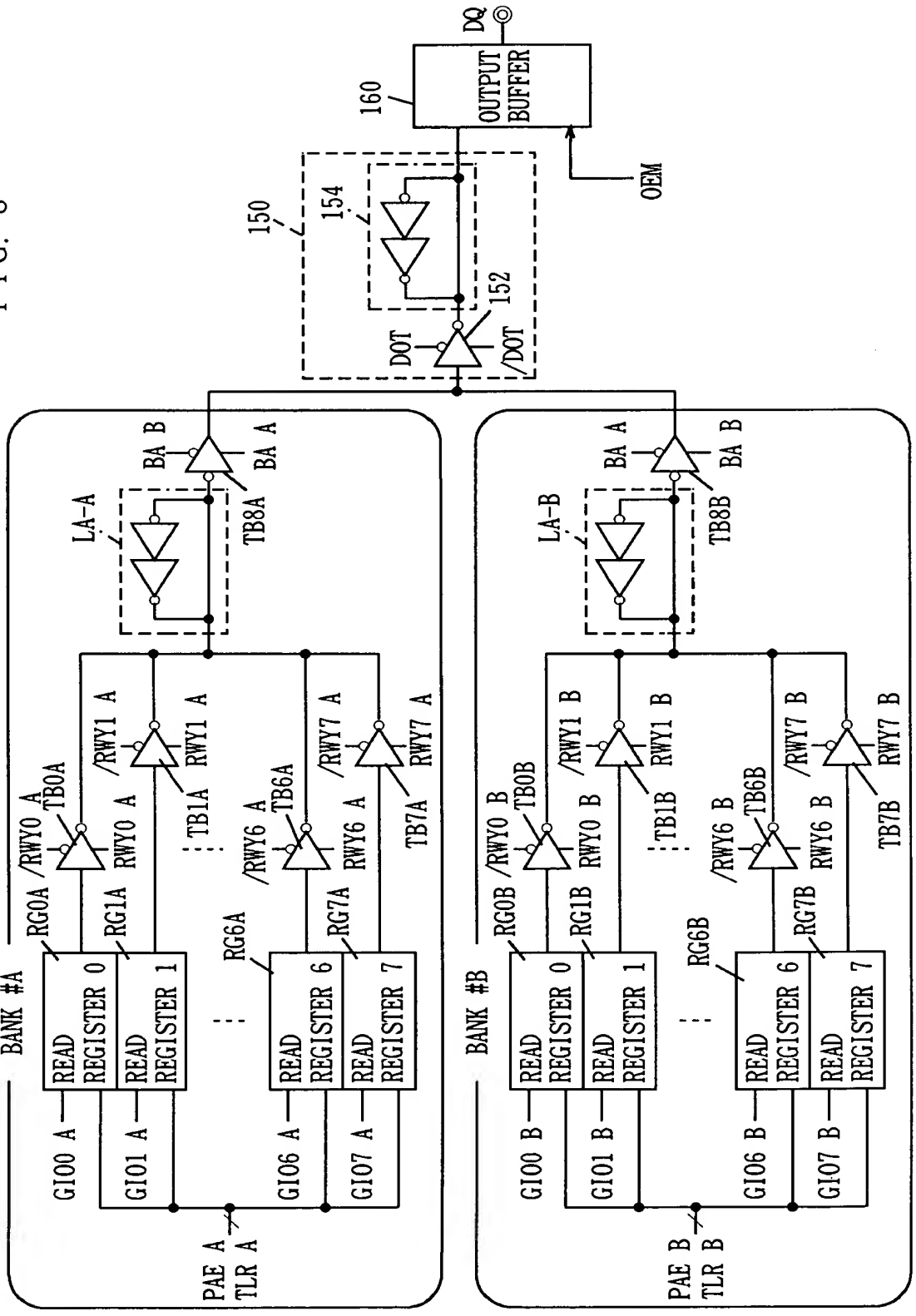

DQ
OUTPUT BUFFER
160
OEM
150
154
152
DOT
/DOT
LA-A
LA-B
BA A
BA B
TB8A
TB8B
BANK #A
BANK #B
/RWY0 A
RWY0 A
/RWY1 A
RWY1 A
/RWY6 A
RWY6 A
/RWY7 A
RWY7 A
TB0A
TB1A
TB6A
TB7A
/RWY0 B
RWY0 B
/RWY1 B
RWY1 B
/RWY6 B
RWY6 B
/RWY7 B
RWY7 B
TB0B
TB1B
TB6B
TB7B
RG0A
RG1A
RG6A
RG7A
RG0B
RG1B
RG6B
RG7B
READ REGISTER 0
READ REGISTER 1
READ REGISTER 6
READ REGISTER 7
GIO0 A
GIO1 A
GIO6 A
GIO7 A
GIO0 B
GIO1 B
GIO6 B
GIO7 B
PAE A
TLR A
PAE B
TLR B

FIG. 9

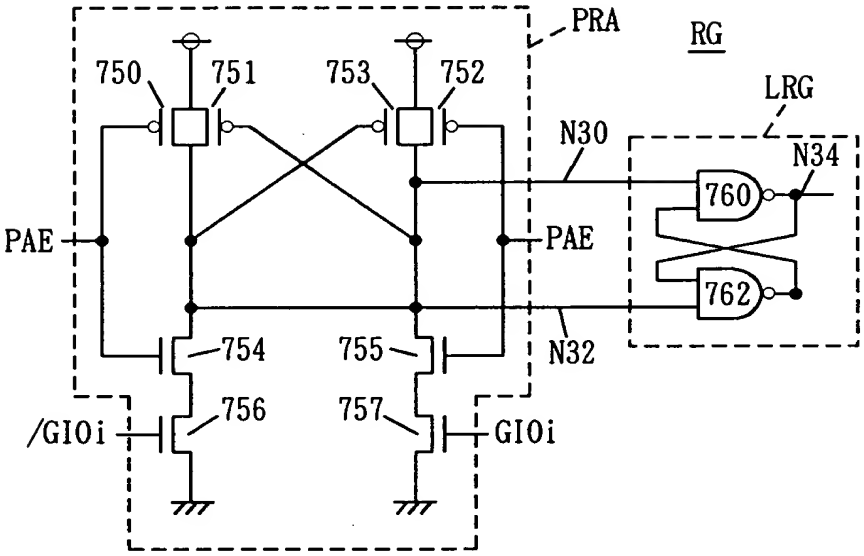

PRA
RG
LRG
750
751
753
752
N30
N34
760
PAE
PAE
762
754
755
N32
/GIOi
756
757
GIOi

FIG. 10

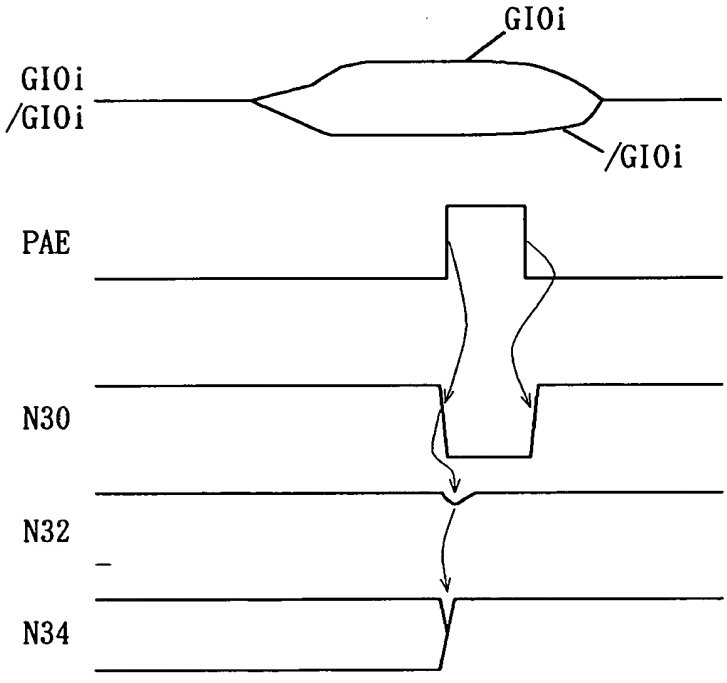

GIOi
GIOi
/GIOi
/GIOi
PAE
N30
N32
N34

FIG. 11

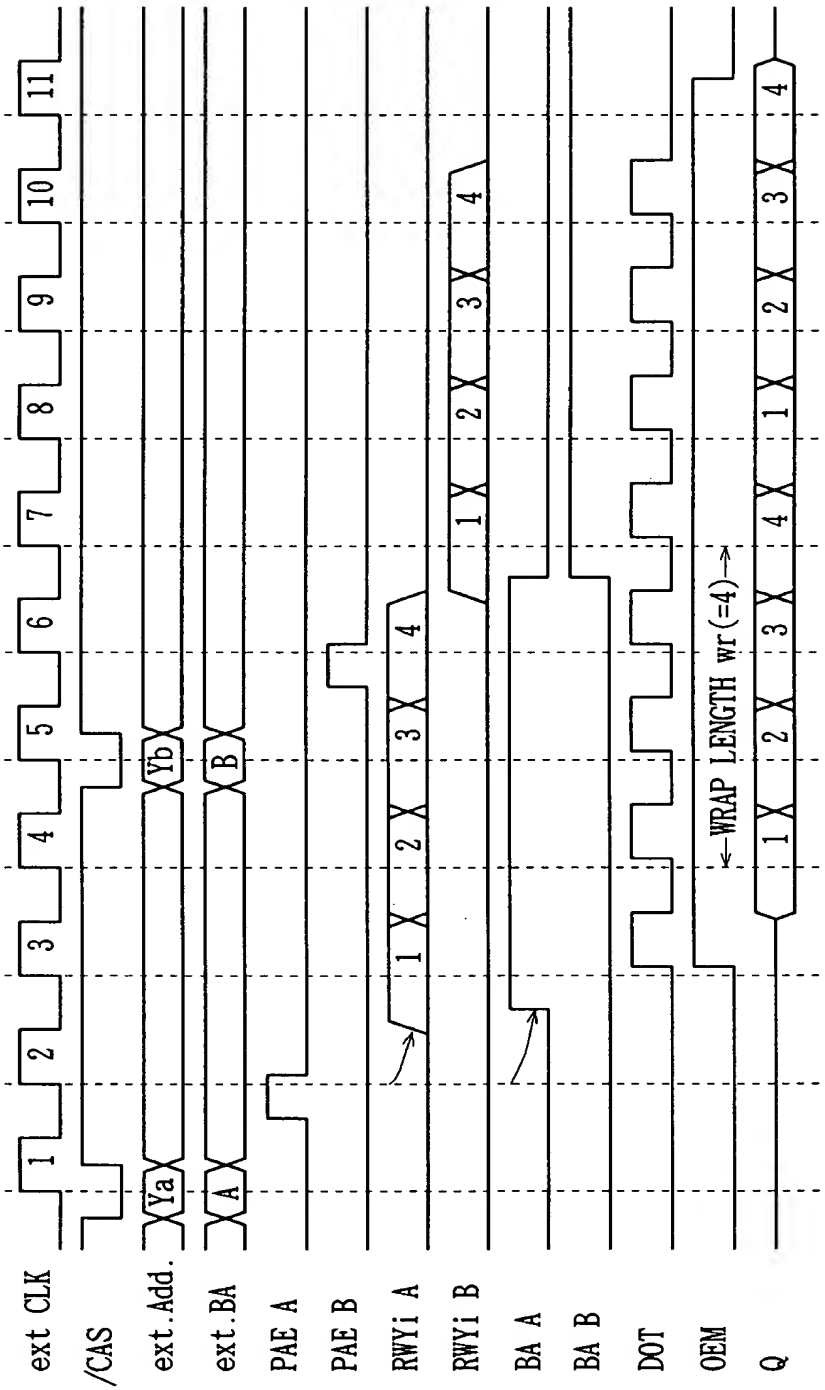

ext CLK
/CAS
ext.Add.
ext.BA
PAE A
PAE B
RWYi A
RWYi B
BA A
BA B
DOT
OEM
Q
1
2
3
4
5
6
7
8
9
10
11
Ya
Yb
A
B
1
2
3
4
1
2
3
4
1
2
3
4
1
2
3
4
←WRAP LENGTH wr(=4)→
LATENCY
la(=3)

FIG. 12

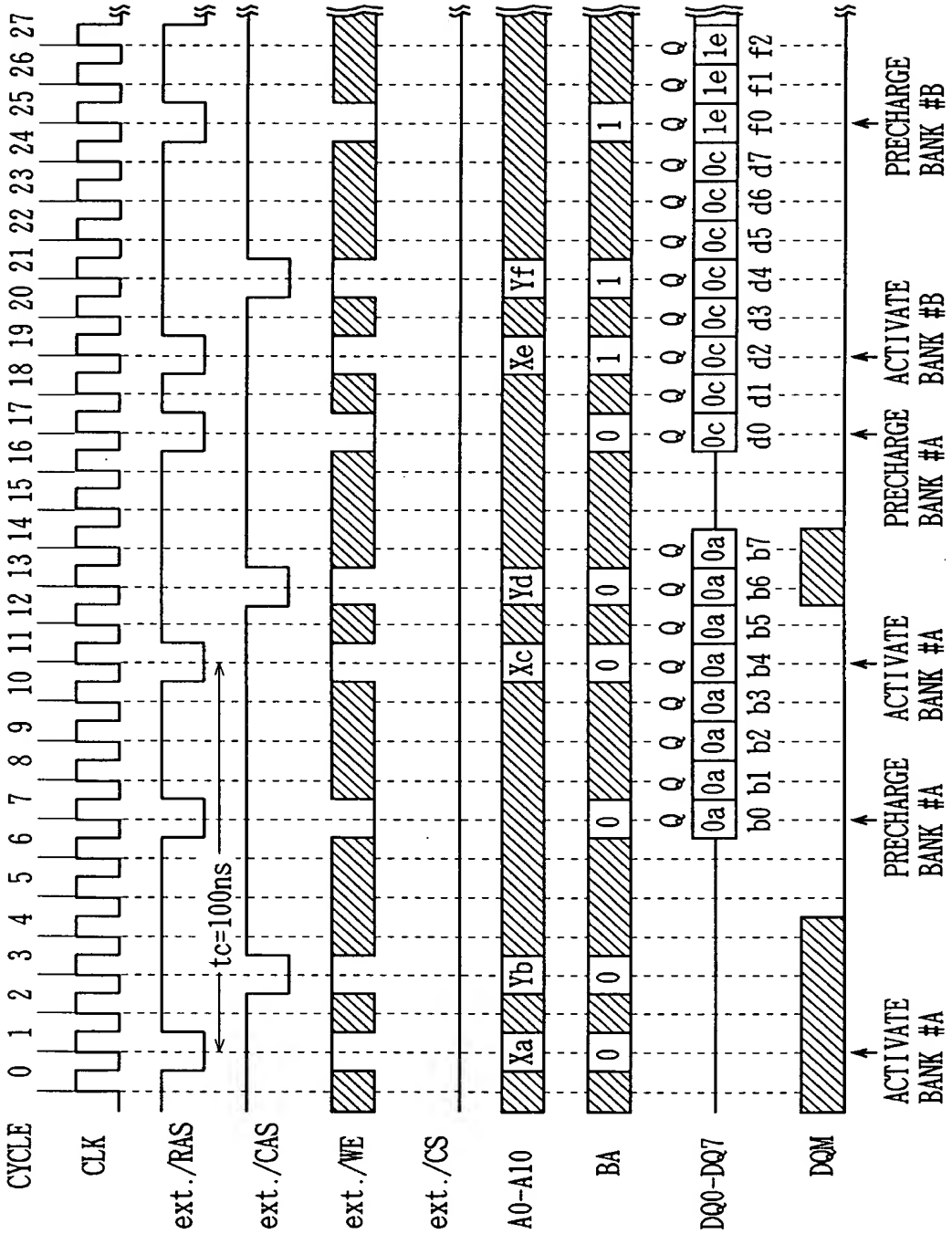

CYCLE
CLK
ext./RAS
ext./CAS
ext./WE
ext./CS
A0-A10
BA
DQ0-DQ7
DQM
tc=100ns
ACTIVATE BANK #A
PRECHARGE BANK #A
ACTIVATE BANK #A
PRECHARGE BANK #A
ACTIVATE BANK #B
PRECHARGE BANK #B

FIG. 13

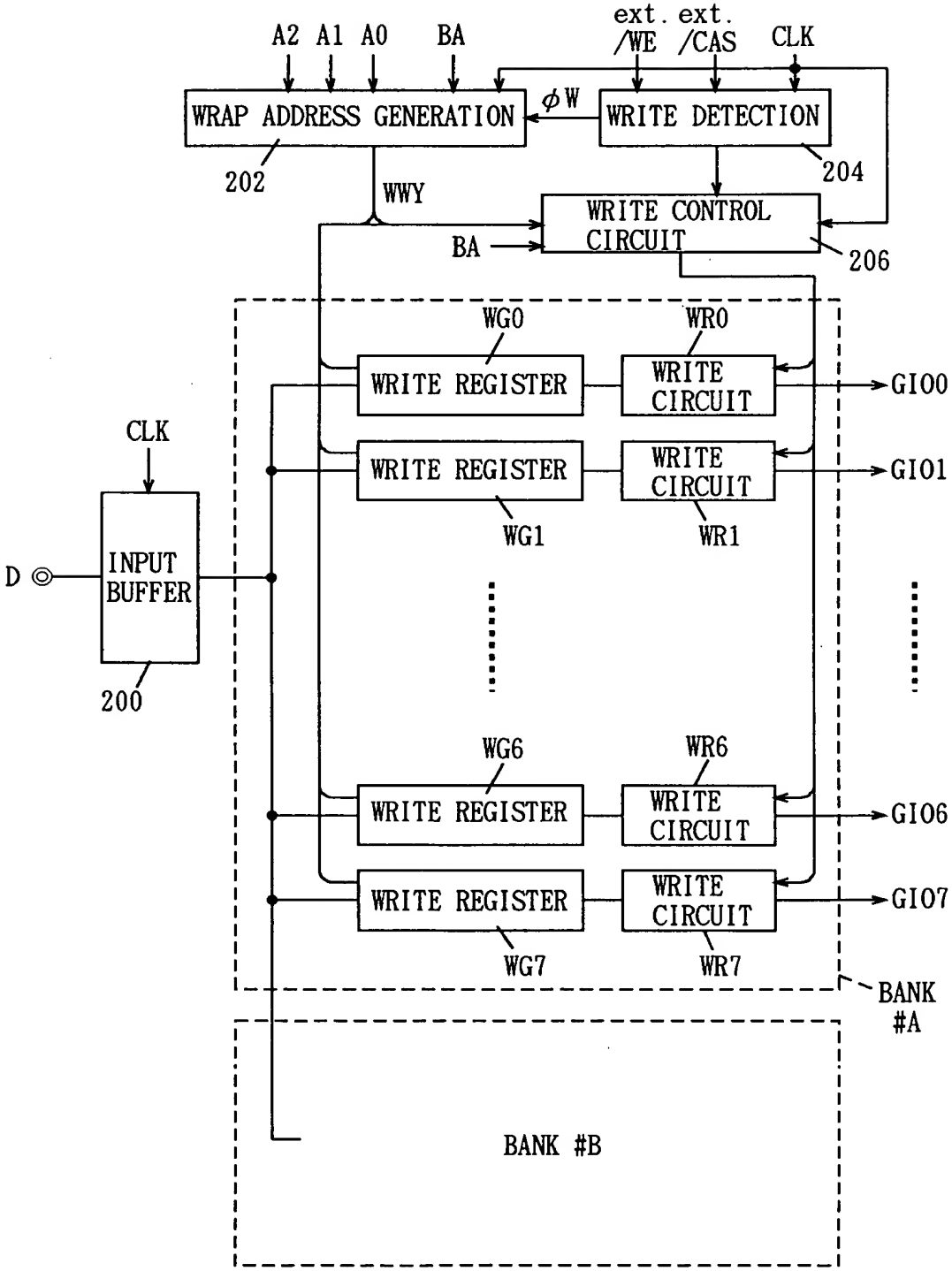

A2
A1
A0
BA
ext. /WE
ext. /CAS
CLK
WRAP ADDRESS GENERATION
φW
WRITE DETECTION
202
204
WWY
WRITE CONTROL CIRCUIT
BA
206
WG0
WR0
WRITE REGISTER
WRITE CIRCUIT
GIO0
CLK
WRITE REGISTER
WRITE CIRCUIT
GIO1
WG1
WR1
D
INPUT BUFFER
200
WG6
WR6
WRITE REGISTER
WRITE CIRCUIT
GIO6
WRITE REGISTER
WRITE CIRCUIT
GIO7
WG7
WR7
BANK #A
BANK #B

FIG. 14

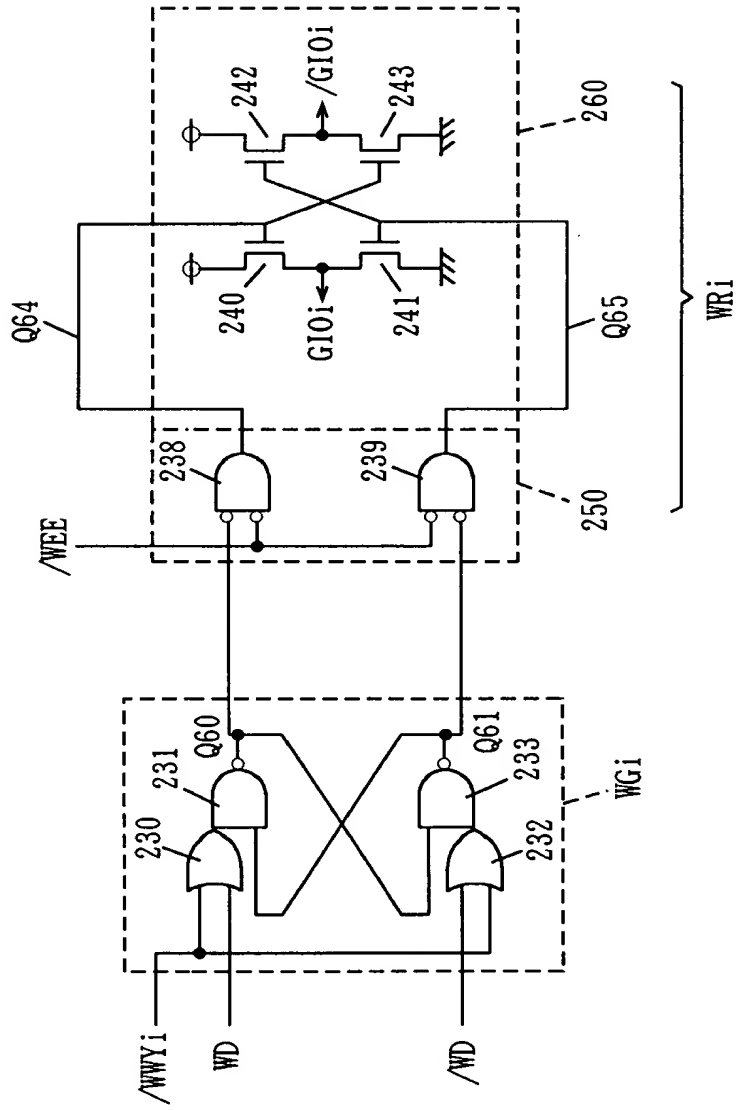

242
/GIOi
243
260
Q64
240
GIOi
241
Q65
WRi
238
239
/WEE
250
Q60
Q61
231
233
WGi
230
232
/WWYi
WD
/WD

FIG. 15

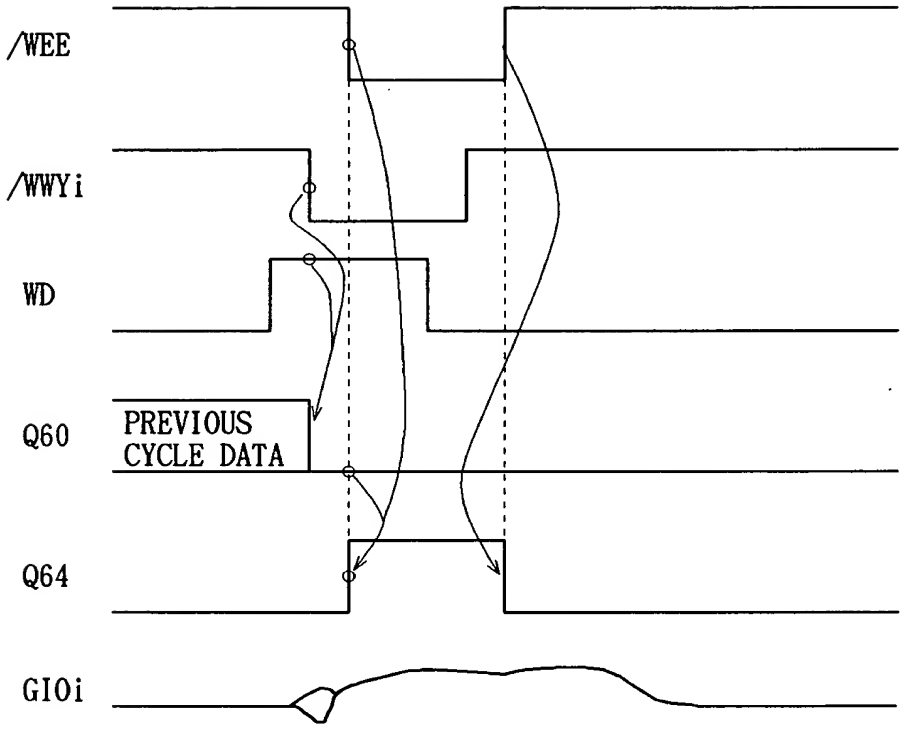


FIG. 16

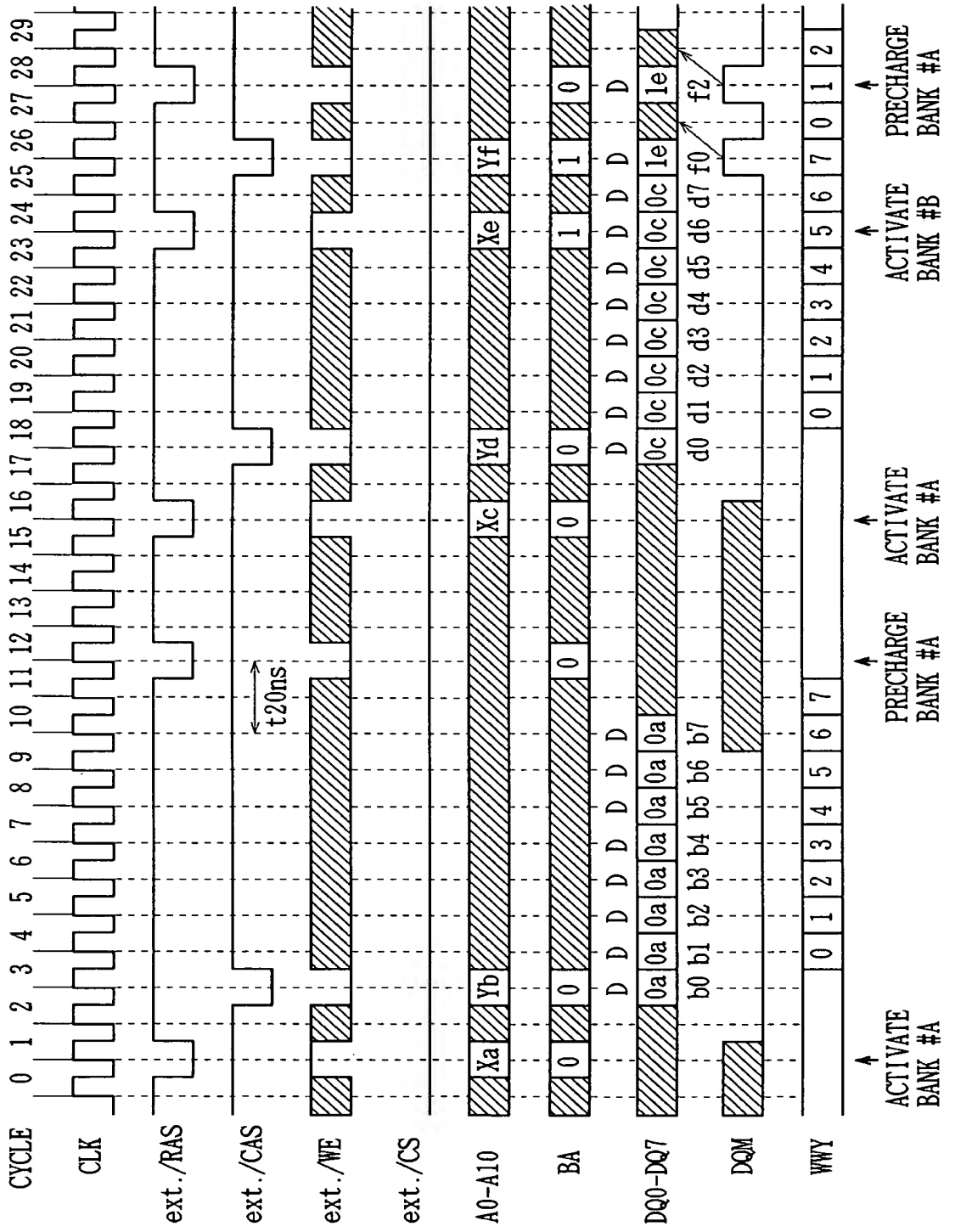

CYCLE
CLK
ext./RAS
ext./CAS
ext./WE
ext./CS
A0-A10
BA
DQ0-DQ7
DQM
WWY
t20ns
ACTIVATE BANK #A
PRECHARGE BANK #A
ACTIVATE BANK #A
ACTIVATE BANK #B
PRECHARGE BANK #A

FIG. 17

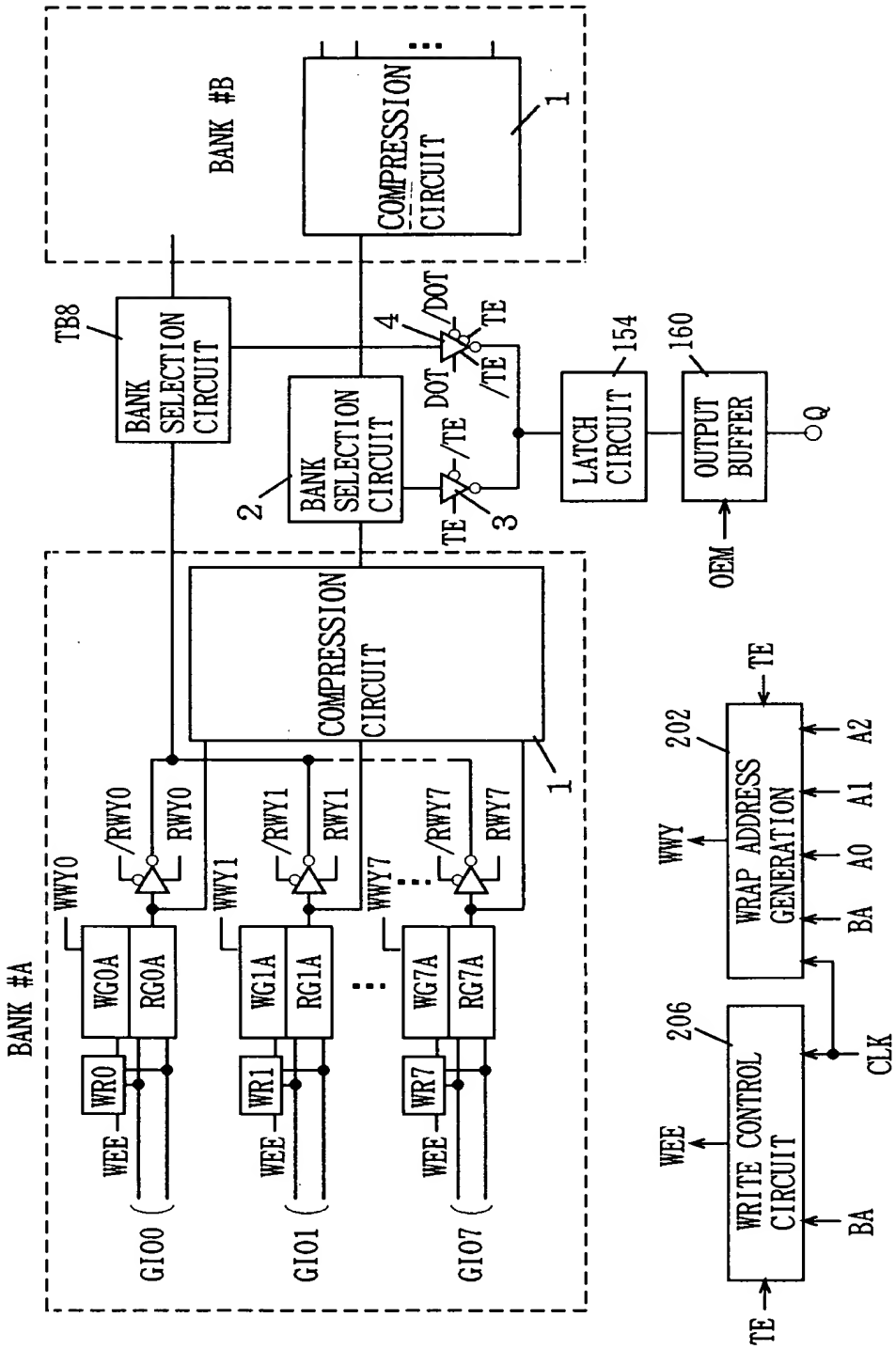

BANK #B
COMPRESSION CIRCUIT
1
TB8
BANK SELECTION CIRCUIT
4
/DOT
TE
DOT
/TE
LATCH CIRCUIT
154
160
OUTPUT BUFFER
Q
2
BANK SELECTION CIRCUIT
/TE
TE
3
OEM
BANK #A
COMPRESSION CIRCUIT
1
WWY0
WWY1
WWY7
/RWY0
RWY0
/RWY1
RWY1
/RWY7
RWY7
WG0A
RG0A
WG1A
RG1A
WG7A
RG7A
WR0
WR1
WR7
WEE
GIO0
GIO1
GIO7
WWY
202
WRAP ADDRESS GENERATION
TE
BA
A0
A1
A2
206
WRITE CONTROL CIRCUIT
CLK
WEE
BA
TE

FIG. 18

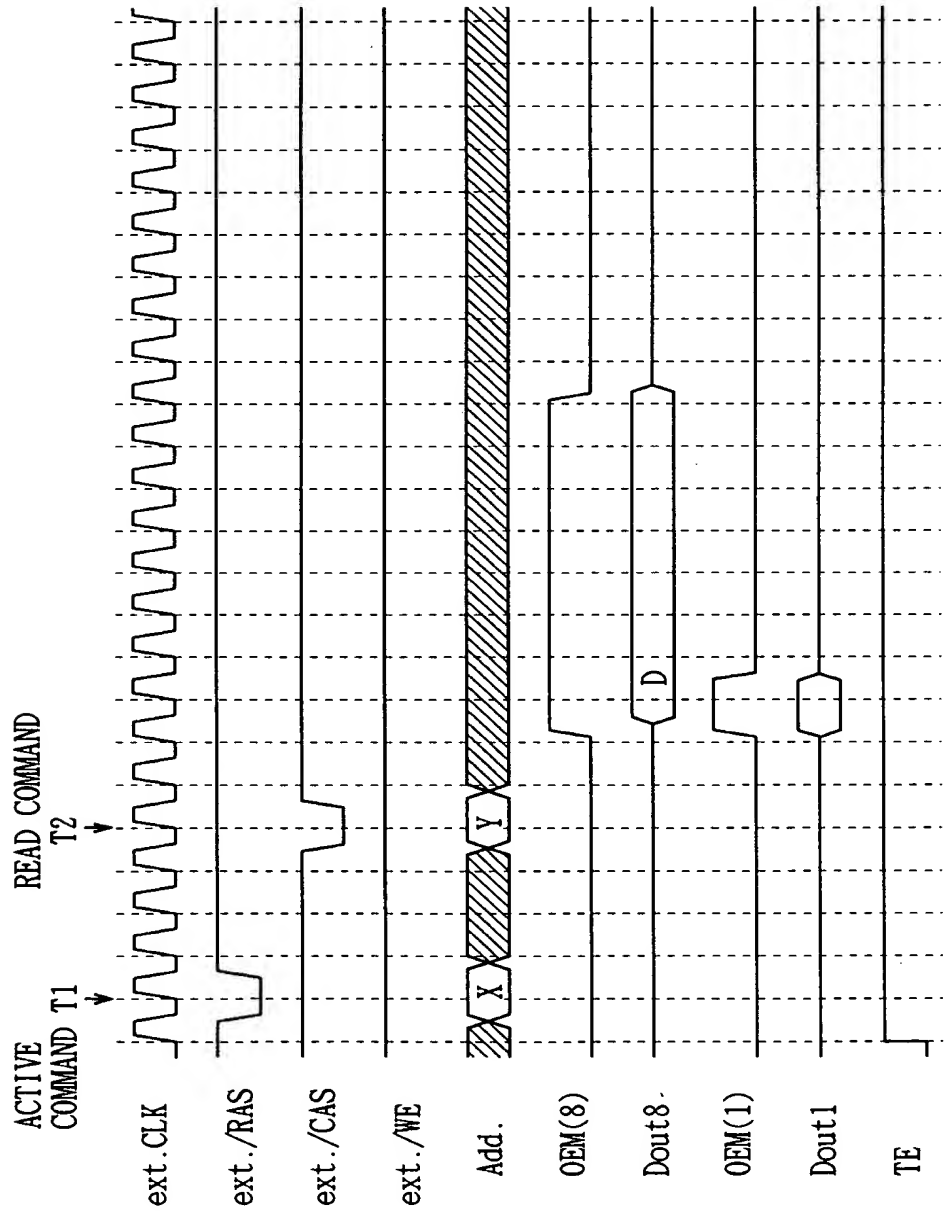

ACTIVE COMMAND T1
READ COMMAND T2
ext.CLK
ext./RAS
ext./CAS
ext./WE
Add.
X
Y
OEM(8)
Dout8
D
OEM(1)
Dout1
TE

FIG. 19

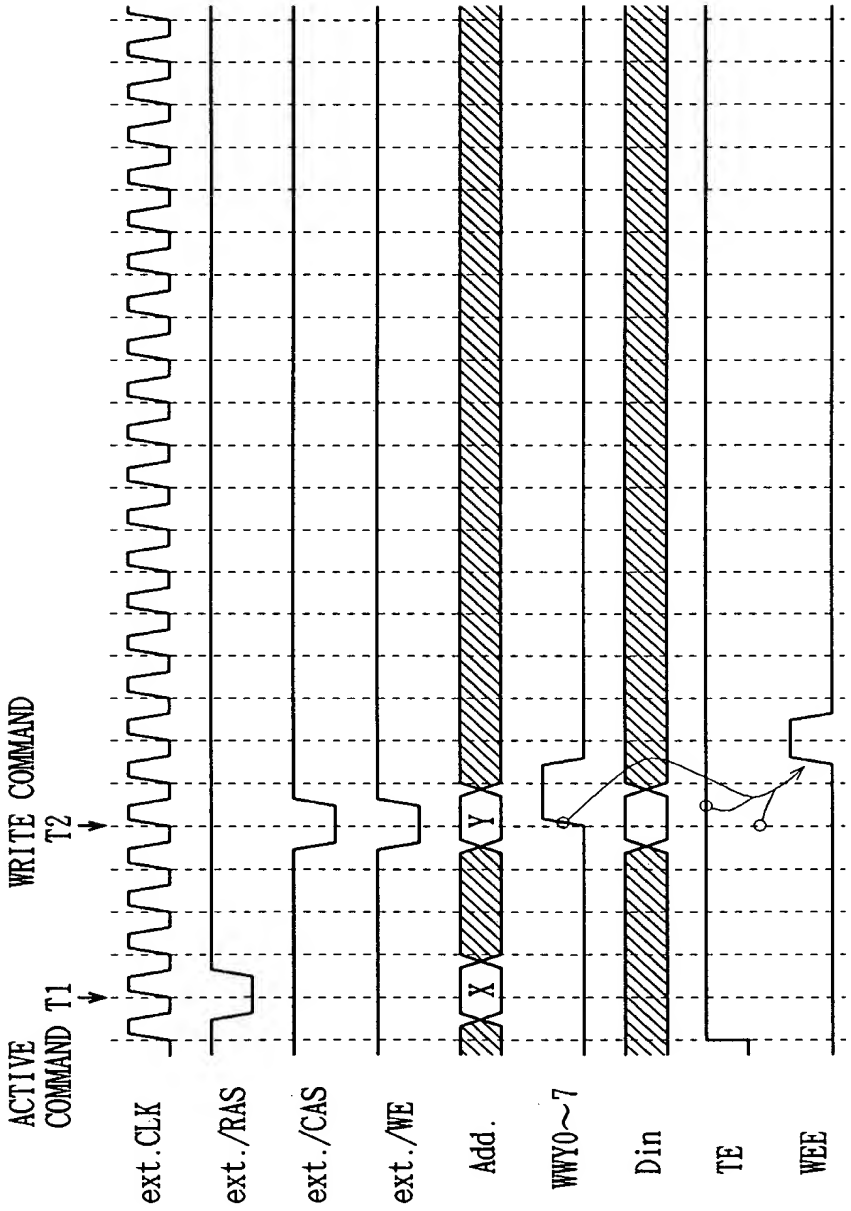

ACTIVE COMMAND T1
WRITE COMMAND T2
ext.CLK
ext./RAS
ext./CAS
ext./WE
Add.
X
Y
WWY0~7
Din
TE
WEE

FIG. 20

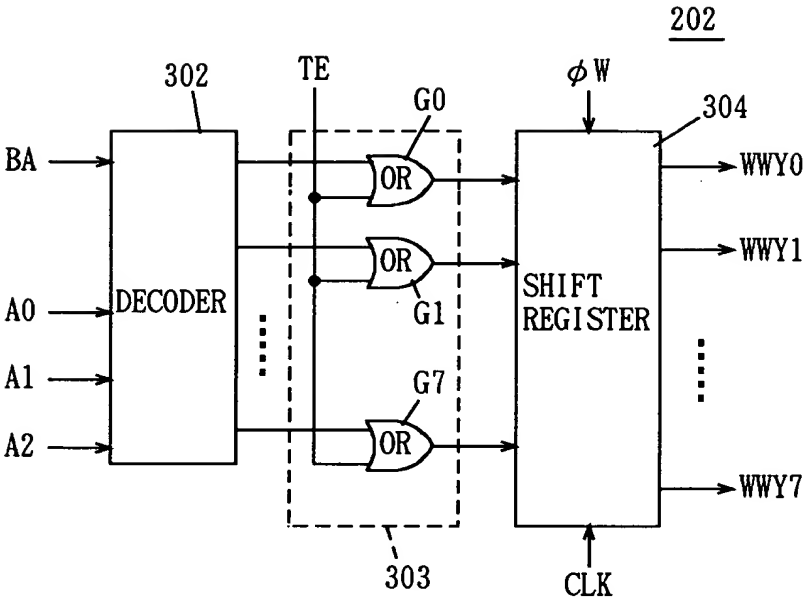

202
302
TE
φW
G0
304
BA
OR
WWY0
OR
WWY1
A0
DECODER
G1
SHIFT
REGISTER
A1
G7
A2
OR
WWY7
303
CLK

FIG. 21

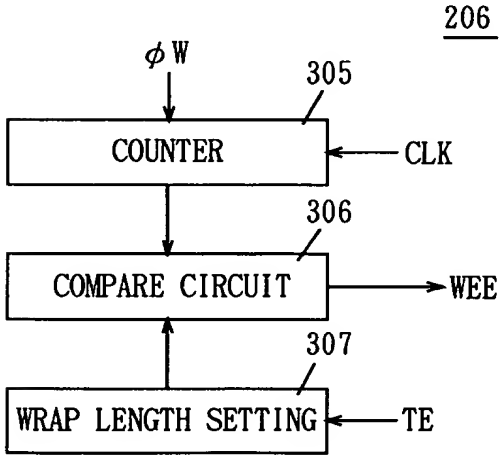

206
φW
305
COUNTER
CLK
306
COMPARE CIRCUIT
WEE
307
WRAP LENGTH SETTING
TE

FIG. 22

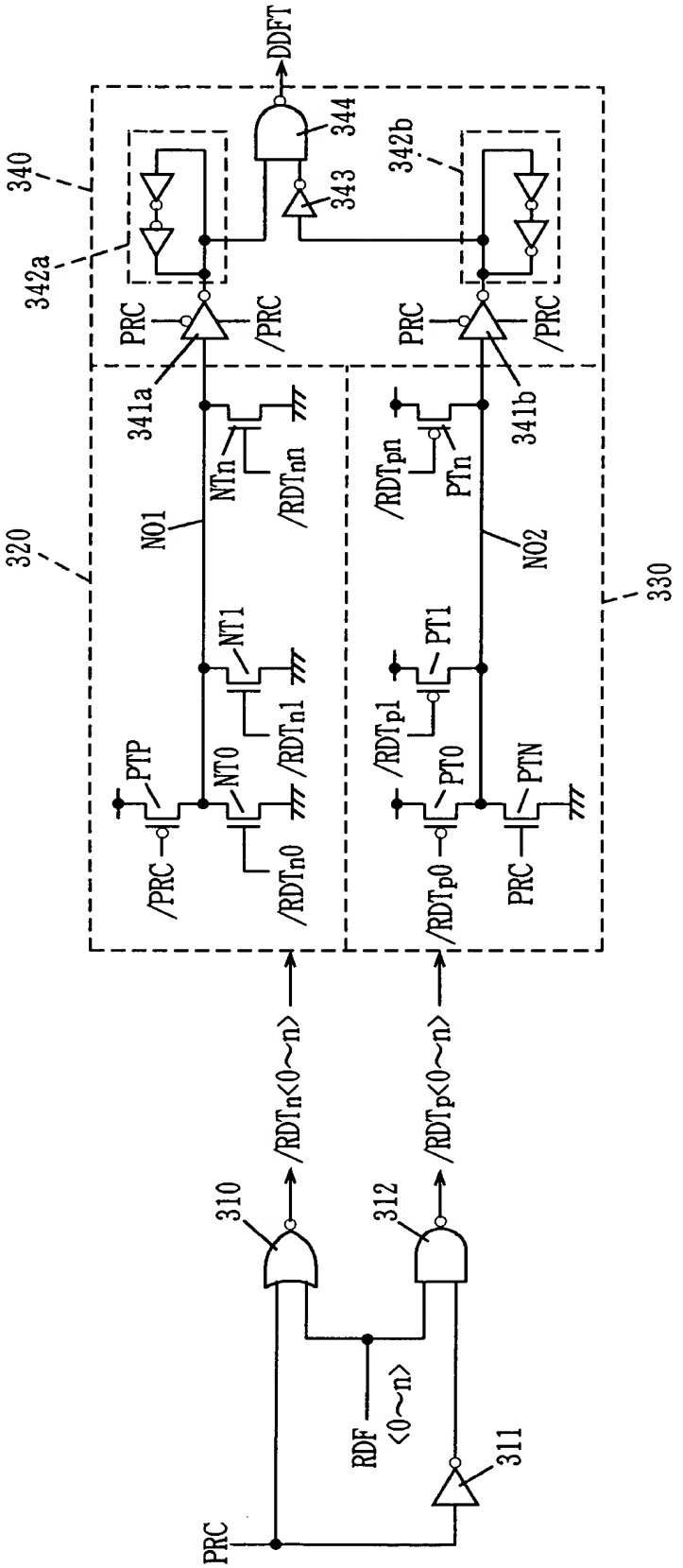

DDFT
340
342a
342b
344
343
PRC
/PRC
341a
341b
320
330
NO1
NO2
NTn
/RDTnn
/RDTpn
PTn
NT1
PT1
/RDTn1
/RDTp1
PTP
NT0
PT0
PTN
/RDTn0
/RDTp0
/RDTn<0~n>
/RDTp<0~n>
310
312
311
RDF
<0~n>
PRC

FIG. 23

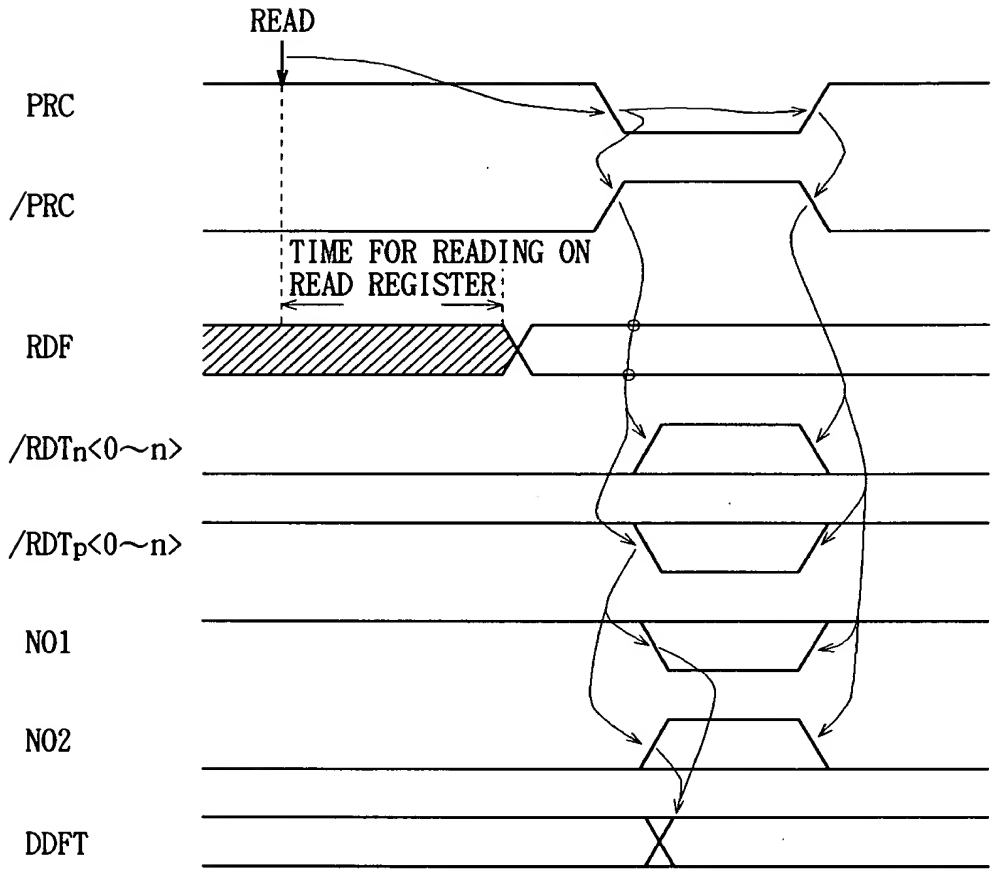


FIG. 24

	/RDT N/P <0:7>	NO1	NO2	DDFT	DECISION
PRECHARGE	L/H	H	L	-	-
ALL "H"	L	H	H	H	PASS
ALL "L"	H	L	L	H	
"H" AND "L"	H & L	L	H	L	FAIL

FIG. 25

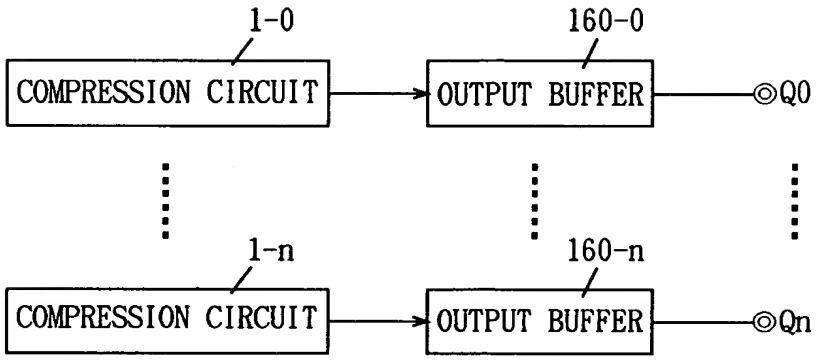


FIG. 26

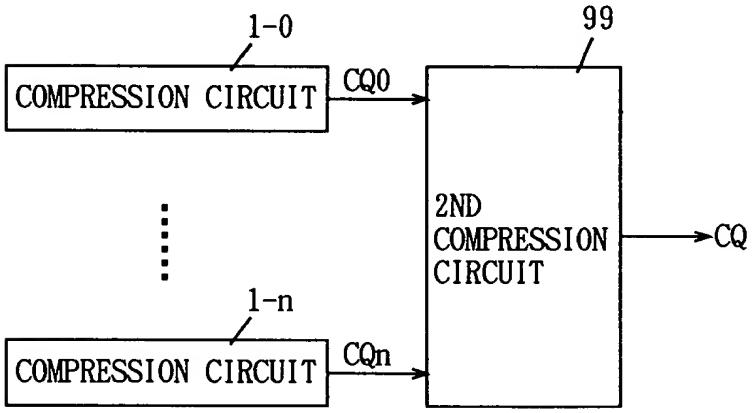


FIG. 27

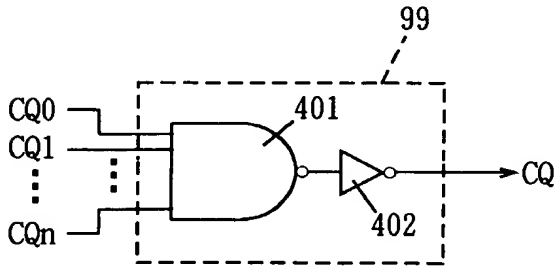


FIG. 28

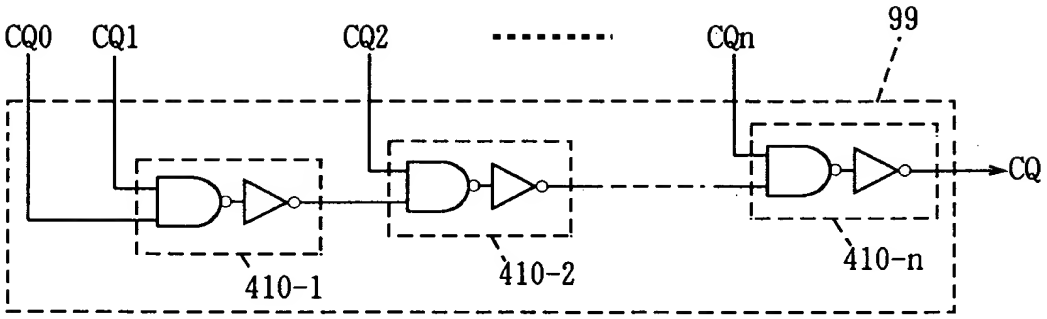

CQ0
CQ1
CQ2
CQn
99
CQ
410-1
410-2
410-n

FIG. 29

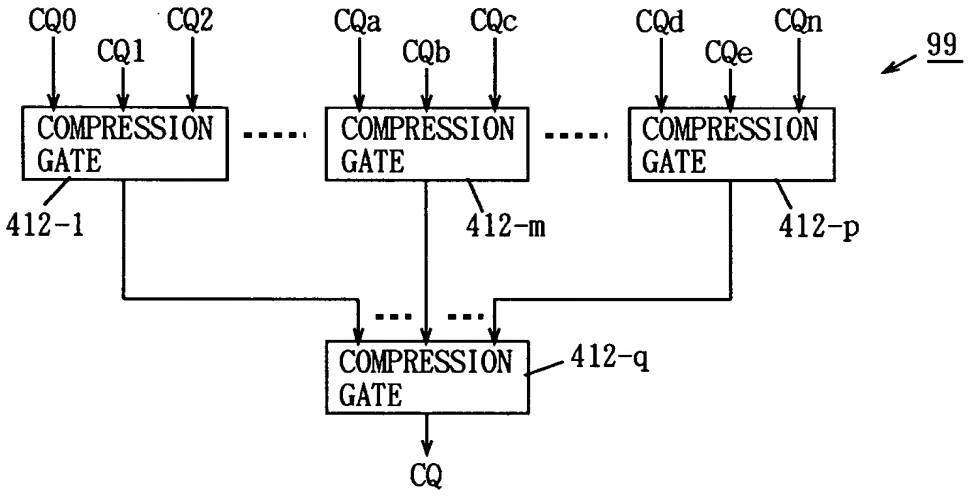

CQ0
CQ1
CQ2
CQa
CQb
CQc
CQd
CQe
CQn
99
COMPRESSION GATE
COMPRESSION GATE
COMPRESSION GATE
412-1
412-m
412-p
COMPRESSION GATE
412-q
CQ

FIG. 30

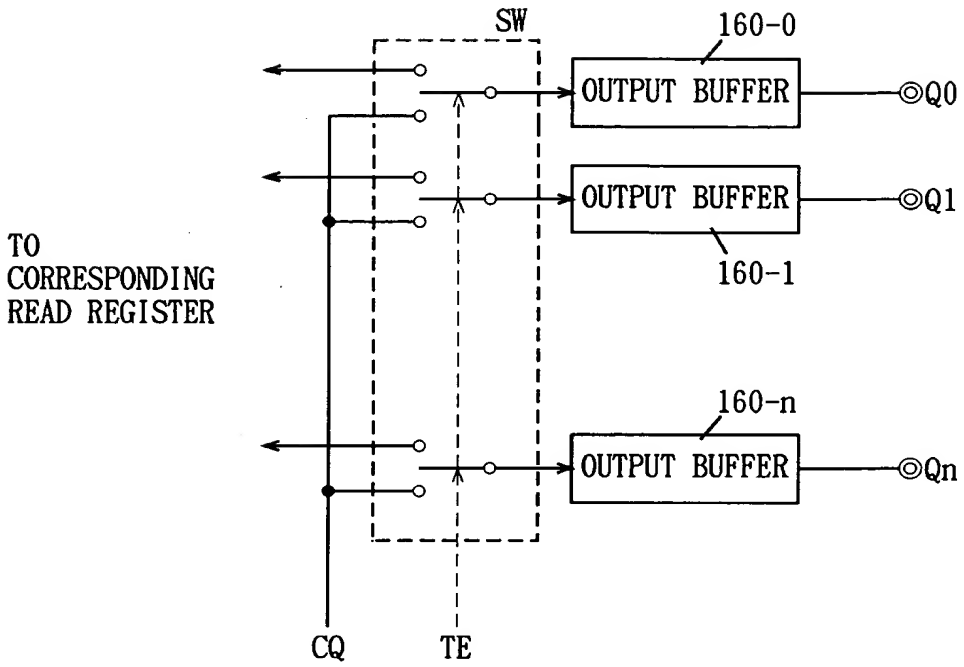


FIG. 31

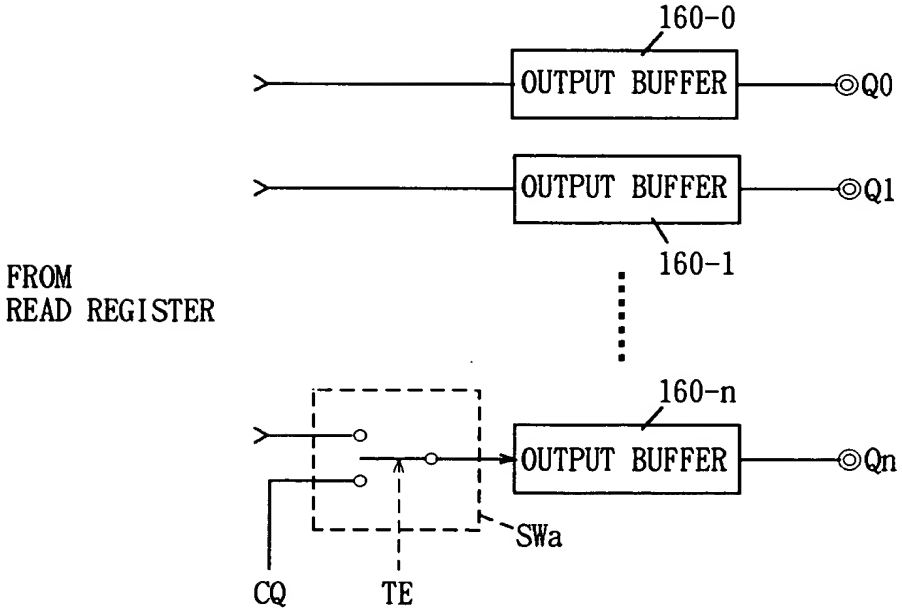


FIG. 32

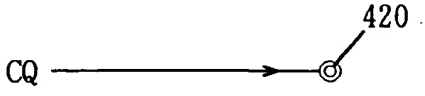


FIG. 33

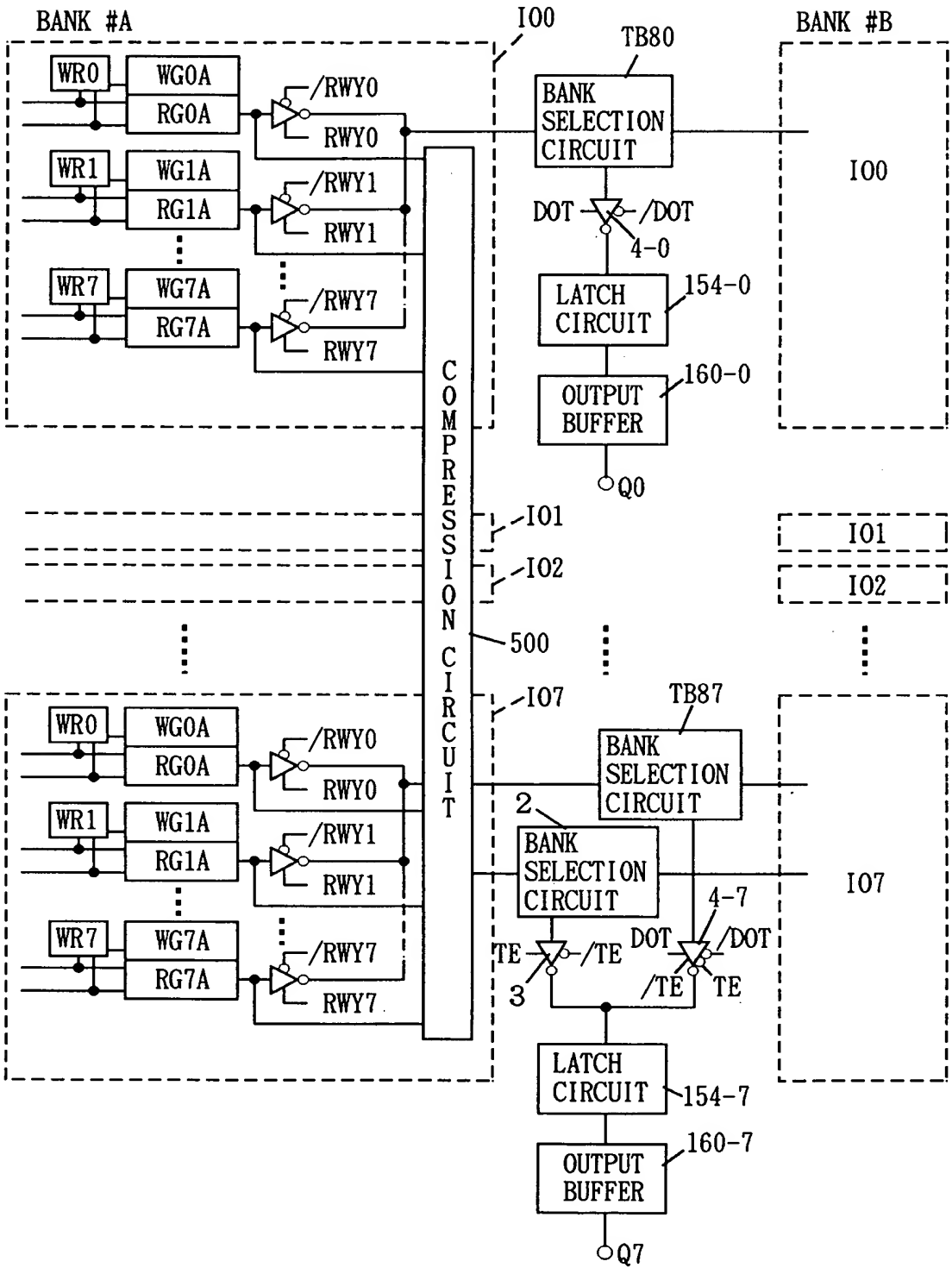

BANK #A
IO0
TB80
BANK #B
WR0
WG0A
RG0A
/RWY0
RWY0
WR1
WG1A
RG1A
/RWY1
RWY1
WR7
WG7A
RG7A
/RWY7
RWY7
BANK SELECTION CIRCUIT
IO0
DOT
/DOT
4-0
LATCH CIRCUIT
154-0
OUTPUT BUFFER
160-0
Q0
COMPRESSION CIRCUIT
IO1
IO2
500
IO7
TB87
2
TE
/TE
3
4-7
LATCH CIRCUIT
154-7
160-7
Q7

FIG. 34

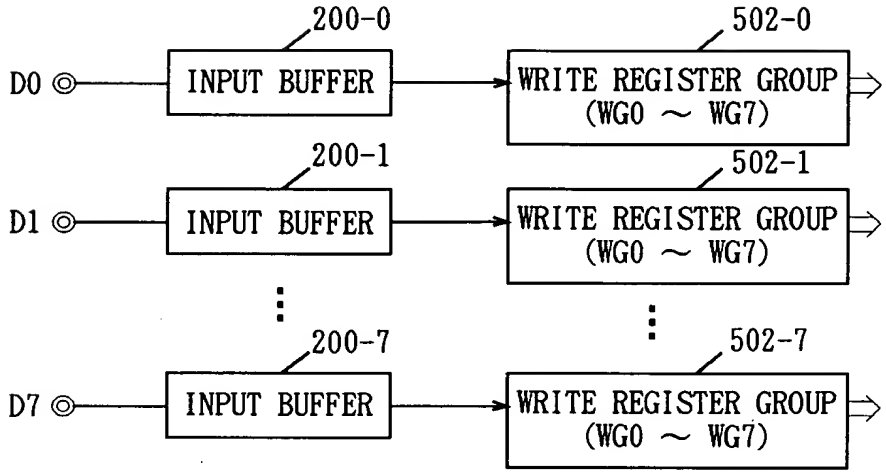

200-0
502-0
D0
INPUT BUFFER
WRITE REGISTER GROUP
(WG0 ～ WG7)
200-1
502-1
D1
INPUT BUFFER
WRITE REGISTER GROUP
(WG0 ～ WG7)
200-7
502-7
D7
INPUT BUFFER
WRITE REGISTER GROUP
(WG0 ～ WG7)

FIG. 35

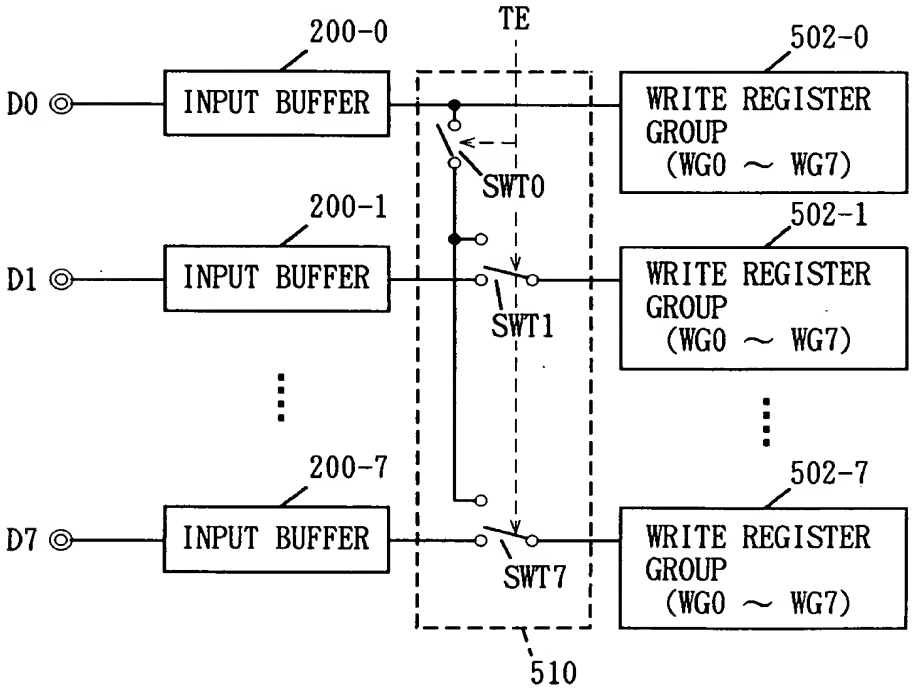

TE
200-0
502-0
D0
INPUT BUFFER
WRITE REGISTER GROUP
(WG0 ～ WG7)
SWT0
200-1
502-1
D1
INPUT BUFFER
WRITE REGISTER GROUP
(WG0 ～ WG7)
SWT1
200-7
502-7
D7
INPUT BUFFER
WRITE REGISTER GROUP
(WG0 ～ WG7)
SWT7
510

FIG. 36

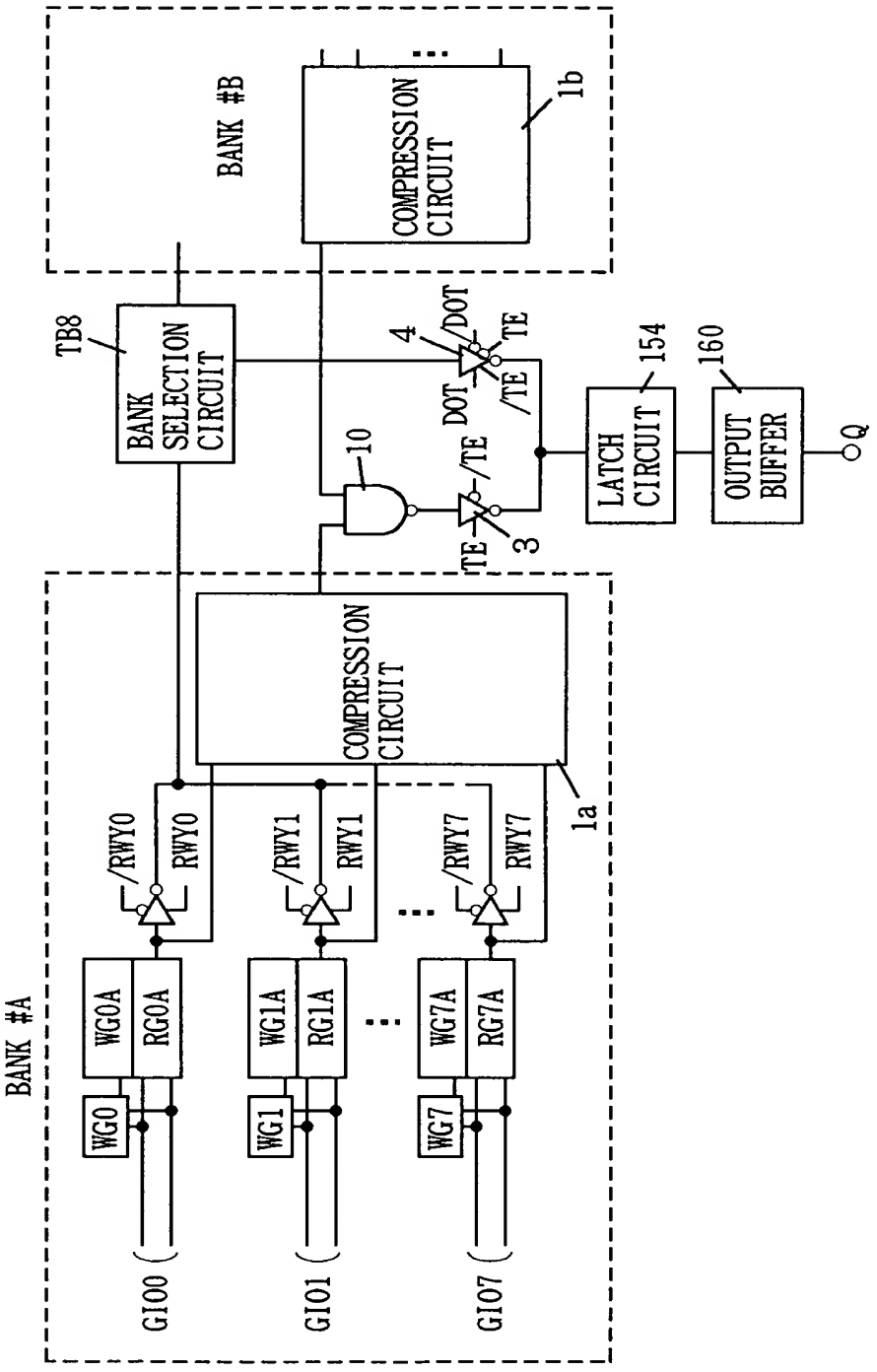

BANK #A
BANK #B
COMPRESSION CIRCUIT
1a
1b
BANK SELECTION CIRCUIT
TB8
10
3
4
DOT
/DOT
TE
/TE
LATCH CIRCUIT
154
OUTPUT BUFFER
160
Q
/RWY0
RWY0
/RWY1
RWY1
/RWY7
RWY7
WG0A
RG0A
WG1A
RG1A
WG7A
RG7A
WG0
WG1
WG7
G100
G101
G107

FIG. 37

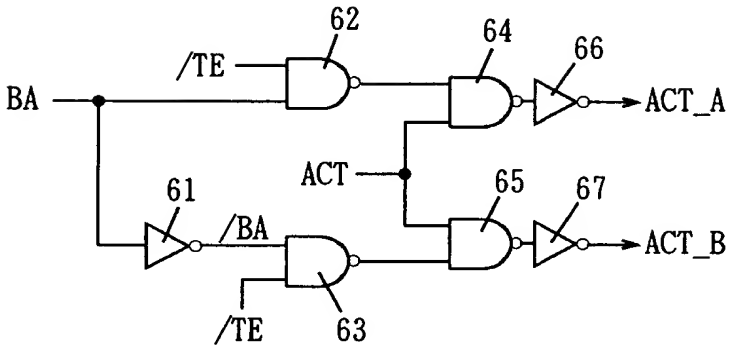


FIG. 38

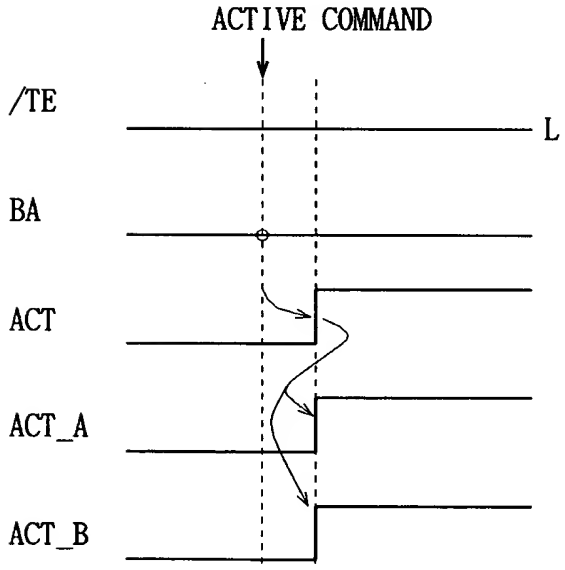


FIG. 39